UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,270	03/27/2001	Ryoichi Inanami	03180.0278	7690

22852 7590 05/26/2006

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,270	INANAMI ET AL.	
	Examiner	Art Unit	
	Phillip A. Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to amendment dated 3-22-2006, wherein claims 1-34 are pending.

Examiners Response to Arguments

2. Applicant's arguments filed 3-22-2006 have been fully considered but they are not persuasive.

Argument 1

Applicant states that, "Kawakami fails to teach or suggest every element in at least independent claims 1, 7,and 15. Specifically, Kawakami fails to teach or suggest a combination including at least "conducting logic synthesis for the CP apertures and) selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," and "conducting logic synthesis again (and) selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns" as recited in independent claims 1, 7, and 15 (emphasis added). Kawakami is silent as to selecting the block pattern based on throughput, and is also silent as to analyzing the degree of frequency again to select the block pattern.

Kawakami thus fails to teach or suggest "conducting logic synthesis for the CP apertures (and) selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," and "conducting logic synthesis again and) selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15."

The applicant is respectfully directed to applicants specification paragraphs [0095], [0101], and [0153]-[0158], which state;

[0095] First, in a step S11, assuming that exposure is performed using a certain aperture 44 and the logic synthesis of the electronic circuit shown in FIG. 9 is performed. In the logic synthesis, the standard cell extraction means 85 shown in FIG. 8 extracts only the cells subjected to CP exposure, i.e., only the standard cells placed on the CP aperture 44. Using the extracted standard cells, the logic synthesis means 86 conducts logic synthesis. At this moment, in the step S1 and the like shown in FIG. 9, the area of a synthesized electronic circuit, the operating frequency of the circuit and the like are designated as design constraints in advance.

[0101] On the other hand, if the step S17 follows, it means that the constraints and the like determination means 87 judges that patterns cannot be synthesized only standard cells arranged on the existing CP apertures 44. Due to this, the standard cell extraction means 85 eliminates the constraint of using only the cells on the CP apertures 44 and the logic synthesis means 86 conducts logic synthesis again.

[0153] First, in the step S11 of FIG. 14, logic synthesis is conducted in the form of a logic expression described in the logic design shown in FIG. 9 using the CP aperture which was manufactured for the device A. At this moment, the area of an electronic circuit to be synthesized, the operating frequency of the circuit and the like are designated as constraints.

[0154] In the step S12, since the number of CP apertures 44 manufactured for the device A is only one, the step S13 follows.

[0155] In the step S13, CP apertures which satisfy the designated constraints are extracted from a synthesized net list.

[0156] In the step S14, it is judged whether or not there is a CP apertures 44 satisfying the constraints if logic synthesis is conducted using only the cells placed on the CP aperture 44. Namely, when designing the device B, logic synthesis is conducted by assuming that the CP aperture 44 to be used was manufactured for the device A. However, it was impossible to generate a net list using only the CP aperture 44 manufactured for the device A. Since the CP aperture 44 manufactured for the device A does not satisfy the constraints, the step S17 follows.

[0157] In the step S17, the constraint of using only the cells on the CP aperture 44 manufactured for the device A is eliminated and logic synthesis is conducted again.

[0158] In the step S18, the number of electron beam shots in case of conducting exposure using the existing CP aperture 44 manufactured for the device A is calculated for the patterns synthesized in the step S17. At this moment, the number of electron beam shots is calculated for the cells placed on the CP aperture 44 to be

used by assuming that CP exposure is conducted and for the other cells and by assuming that VSB exposure is conducted. That is to say, the number of shots is calculated by assuming that among the standard cells used in the circuit, the cells placed on the CP aperture 44 manufactured for the device A are subjected to CP exposure and that the other cells are subjected to VSB exposure. As a result, it is found that the number of shots is 4.90 M shots per chip.

The examiner has interpreted that, support for the limitation "conducting logic synthesis again", as recited in claims 1,7, and 15, is believed to be provided by the applicants references above, and that the subject limitation refers to the steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device B. In other words, after device A is designed the constraints used for device A are reviewed in preparation for logic synthesis of device B, and if the system decides the standard cell arrangement (constraint) for device A cannot be used for device B, then it is turned off and logic synthesis of device B is performed independent of the standard cells selected for the logic synthesis of device A.

The applicant is respectfully directed to Kawakami (544), Column 4, line 1-19, which states; The block mask 20 is limited to about 100 block patterns 42 in the mask area 41 which are selectable without movement as shown in FIG. 3. Therefore, the problem is which block pattern is to be used. The layout data 54 for the IC designed has patterns of the layers in hierarchical structure. By analyzing each layer, a plurality of repetitive patterns are extracted, and out of these patterns, a block pattern 42 to be

arranged in the mask area 41 is selected taking into consideration the frequency of repetition. Further, the place where the selected block pattern 42 is to be arranged in the mask area 41 is determined taking the frequency, etc. into consideration. After that, in accordance with the system restraint information, the mask restraints 56 and the mask-related process setting information (mask) 57, the line width of the block pattern 42 is determined thereby to produce the mask layout 60. Based on this mask layout 60, the block mask 20 is produced. For the remaining mask areas 41, a layer exposed in the next process or the block pattern used for the device next to be produced is provided.

Also Column 9, line 55-67; and Column 10, line 1-23, which state; In step 101, the basic elements (cells) are designed in a cell design process 51 taking into consideration the design rule, the strategy, the device performance and the restraints in the electron beam exposure apparatus. The data related to various types of cell designed are stored in a cell library 52.

In step 102, the cells stored in the cell library 52 are combined in the device design process 53, and by wiring between them, layout data 54 corresponding to each device is produced. According to this embodiment, assume that a system LSI is to be designed and fabricated. For the system LSI, the basic configuration including a CPU core, a logic circuit, a memory and analog circuit is prepared in advance, and the range of application of these elements is changed or the wiring thereof is set as a designing process.

Specifically, a multiplicity of devices are designed from a single cell library 52 thereby to produce a group 70 including a plurality of layout data 54.

In step 103, the plurality of layout data 54 in the group 70 is analyzed in the layout analysis process 74 and, by counting the frequency at which each cell is referred to, producing the cell reference frequency information (cell-to-mask change priority information) 75. This information indicates the order of priority in which the cells are changed to masks.

In step 104, the process for converting the basic elements (cells) to block patterns is performed in the cell-to-block conversion process 73. First, by reference to the cell reference frequency information 75 and the system restraint information/mask restraints 72, the cells to be changed to masks are determined thereby to produce a mask layout A76. In the process, with reference to the design setting information/ object layer/design shift 71 containing information such as the object layer and the design shift value and the system restraints/mask restraints 72 constituting information mainly on the restraints of the block mask pattern, it is determined whether conditions of a block pattern are met by the pattern of a specific layer of the cell to be changed to a mask. In the case of a complicated cell, for example, the cell pattern is so large that it may not be encased in the block pattern. In such a case, the cell pattern is formed with a plurality of block patterns by such process as segmentation. In the final step, the process shift information and dose information for changing the line width in accordance with the process are added to the mask layout A76.

The examiner has interpreted from a comparison of the applicants and the Kawakami (544) references above that, both perform multiple device design layouts using a stored standard cell library, and neither the applicant nor Kawakami (544) constrain the design of subsequent devices to standard cell layouts previously selected for any other prior device design; i.e., when "conducting logic synthesis again", as recited in claims 1,7, and 15.

Argument 2

Applicant states that "Kawakami also fails to teach or suggest a combination including at least "recording the standard cell library ... on said CP apertures related to the standard cells" as recited in claims 1,7, and 15. Kawakami only teaches that, layout data are produced by combining the cells stored in a cell library (column 7, lines 58 - 66). However, Kawakami fails to teach that cells stored in the cell library are placed on the aperture. In Kawakami, the cells to be placed on the aperture are determined to produce a mask layout by reference to the cell reference frequency in the layout data, and apertures are not selected before layout data is produced. Kawakami thus fails to teach or suggest at least, "recording the standard cell library ... on said CP apertures related to the standard cells," as recited in claims 1, 7, and 15 (emphasis added)."

The applicant is also respectfully directed to Kawakami (544), Column 3, line 46-54 and Column 4, line 9-19, which state; The cells are designed in advance by the cell design means 51 taking the restraints in design rule, strategy, device performance and the exposure unit into consideration, and are stored in a cell library 52. In the device

design means 53, the cells are arranged with reference to the cell library 52 and wiring is laid between the cells thereby, to design the desired device, and is stored as layout data 54. The cell library 52 is the basic resource and is used repeatedly for designing several types of device layout.

Further, the place where the selected block pattern 42 is to be arranged in the mask area 41 is determined taking the frequency, etc. into consideration. After that, in accordance with the system restraint information, the mask restraints 56 and the mask-related process setting information (mask) 57, the line width of the block pattern 42 is determined thereby to produce the mask layout 60. Based on this mask layout 60, the block mask 20 is produced. For the remaining mask areas 41, a layer exposed in the next process or the block pattern used for the device next to be produced is provided.

The examiner has interpreted from the Kawakami (544) references above, that the standard cells are previously stored in the cell library and arranged on a mask area 41, which is a CP aperture, as recited in claims 1,7, and 15.

3. The subject rejection in the office action mailed on 12-22-2006 is attached below.

Claims Rejection – 35 U.S.C. 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was

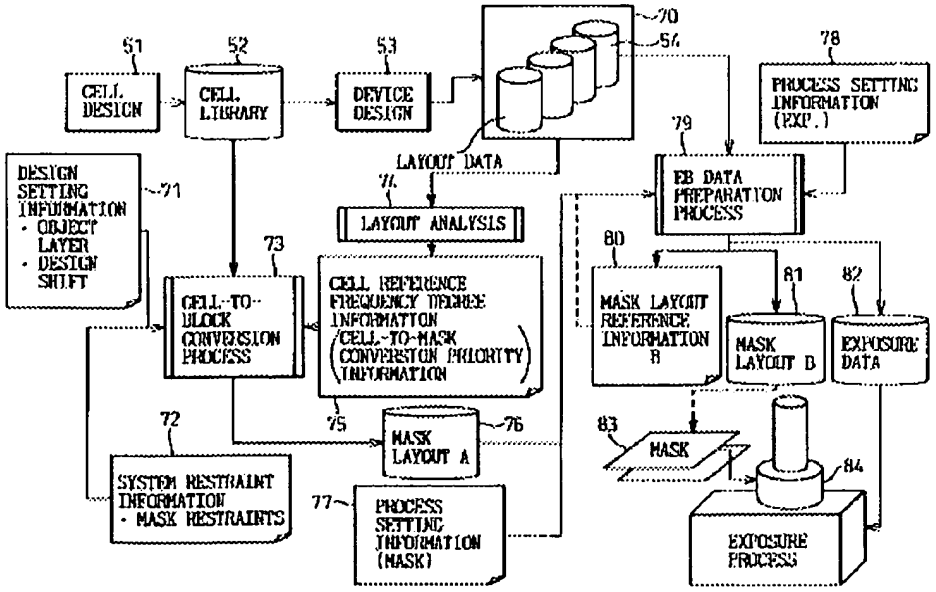
made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-34 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,546,544 to Kawakami, in view of Hoshino, U.S. Patent No. 6,225,025.

Kawakami (544) discloses a method of producing a mask for electron beam fabrication of an integrated circuit that include the following;

(a) Producing mask data, where block (CP) apertures are selected via cell design process 51, which uses a basic element (standard cell) library 52, and device design means 53, to arrange (place) the cells and the wiring between the cells thereby, designing (logic synthesis) the desired device, which is stored as layout data 54 , as recited in claims 1,7,9,12-15,18,24,28,32, and 34. See Column 3, line 35-65; Column 7, line 48-67; Column 8, line 1-7; and Figure 5 below;

Fig.5

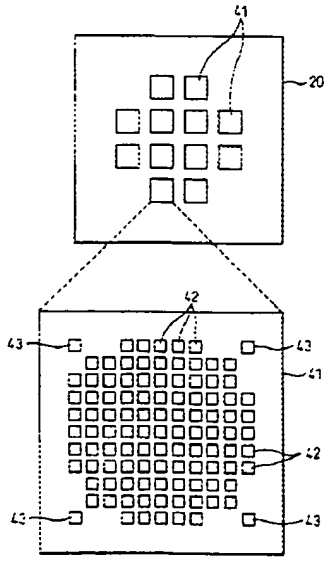


(b) Selecting variable beam (VSB) for exposing the wiring between cells, to be carried out separately with variable rectangle apertures; i.e., without using the basic (standard) cell apertures, as recited in claims 1,2,5,7,8,15,16, and 26. See Column 2, line 60-67; Column 3, line 1-10; and Column 6, line 1-12.

(c) Determining placement and routing (layout) of the mask blocks (apertures), based on frequency of use to maximize throughput, as recited in claims 1,6,7,15,11, 19, and 21. See Column 3, line 50-67, Column 4, line 1-26; Column 6, line 13-25; and Column 8, line 8-28;

(d) The block mask 20 is limited to about 100 block patterns 42 in the mask area 41 which are selectable without movement as shown in FIG. 3. Further, in accordance with the mask layout 60, the exposure data 61 including the block pattern select information and the corresponding information on deflection position is produced and stored, as recited in claims 3,7, and 15. See Column 4, line 1-26; and Figure 3 below;

Fig.3



(e) If fully efficient exposure is not possible a new mask is created, as recited in claims 10,18,23, and 31. See Column 9, line 55-67; and Column 10, line 1-4.

Kawakami (544) as applied above fails to teach the use of standard cells on CP apertures listed in an order of frequency of use according to a difference between a VSB shot number and a CP shot number, as recited in claims 20-23,25,27,29-31, and 33. However, Hoshino (025) discloses a method of fabricating semiconductor devices with electron beam lithography that utilizes mask's having block (CP) apertures formed using shot number analysis based on frequency of use (See Figure 34 below; and Column 11, line 41-54). In addition, the results of the shot number analysis are presented graphically (See Figure 37 below) showing the shot count difference between VSB and block (CP) selection, as recited in claims 20-23,25,27, 29-31, and 33. See Column 19, line 60-67; Column 20, line 1-45; Figure 34; and Figure 37 below.

FIG. 34

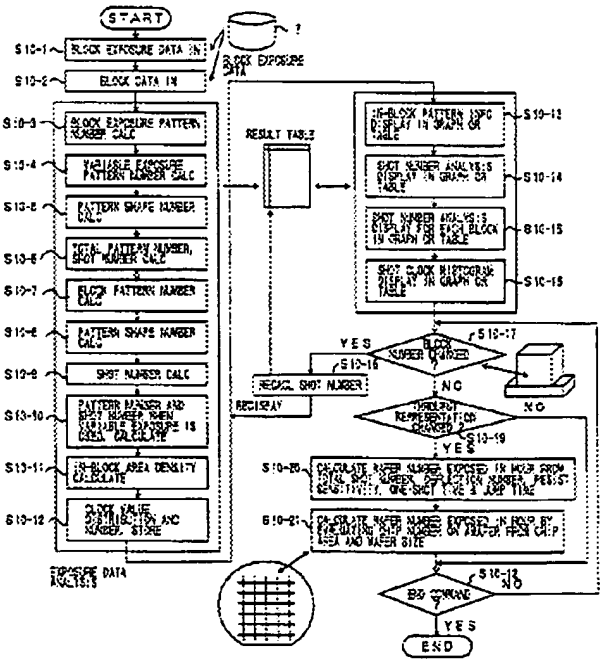
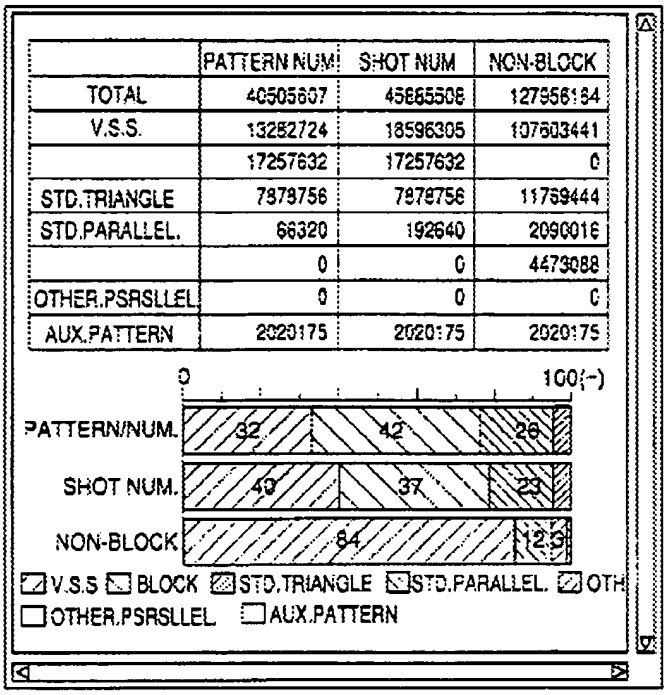


FIG. 37



	PATTERN NUM.	SHOT NUM	NON-BLOCK
TOTAL	40505607	45665508	127556184
V.S.S.	13252724	18596305	107603441
	17257632	17257632	0
STD.TRIANGLE	7979756	7979756	11759444
STD.PARALLEL.	66320	192640	2090016
	0	0	4473088
OTHER.PSRSLLEL	0	0	0
AUX.PATTERN	2020175	2020175	2020175

Therefore it would have been obvious to one of ordinary skill in the art that the cell projection lithography apparatus and method of Kawakami (544) can be modified to use the shot analysis of Hoshino (025), to provide a method for discriminating between exposure patterns exposed according to different exposure processes, such as a variable-beam exposure process, and a block exposure process, thereby the number of shots in the exposure is reduced sharply, and the throughput of exposure is improved substantially.

Conclusion

6. The Amendment filed on 3-22-2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the references cited in the Office Action mailed 12-22-2005.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 6:30 am to 3:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nikita Wells

NIKITA WELLS
PRIMARY EXAMINER

PJ
May 18, 2006